RICHARD ELMS
SUPERVISORY PATENT EXAMINER
FECHNOLOGY CENTER 2800

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DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on February 26, 2004 and the Information Disclosure Statement filed July 19, 2004.

2. Claims 1 - 20 are pending in this case. Claims 1, 10, and 15 are independent claims.

Information Disclosure Statement

3. The IDS filed on 07/19/04 has been considered.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. lannucci Robert on December 14, 2004.

The application has been amended as follows:

Abstract, line 2 changes "comprises" To - -includes- -

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Claim 1, line 13 changes "atching" To - -latching- -

Claim 14, line 2 changes "voltageduring" To - -voltage during- -

Allowable Subject Matter

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- 6. Claims 1 20 are allowed.
- 7. The following is an examiner's statement of reasons for allowance:

With respect to claims 1 and 10, in addition to other elements in the respective claim, the prior art does not teach or suggest "a verify-program device arranged for saving a datum in one of the memory cells by repeating a verify-program cycle until the datum is saved in the memory cell, without exceeding N cycles, the verify-program cycle including reading the memory cell then applying a pulse of a programming voltage to the memory cell if the datum to be saved has a program logic value and if the datum read in the memory cell has an erase logic value; an erase verify device arranged for: supplying an erase verify signal having a determined value when the datum read in a memory cell during the first verify-program cycle of an operation of programming the memory cell, has an erase logic value; and latching the erase verify signal before applying the first pulse of programming voltage to the memory cell".

With respect to claim 15, in addition to other elements in the respective claim, the prior art does not teach or suggest "a first verify-program device having a first input connected to receive an input datum, a second input connected to the output of the first read circuit, and an output that supplies a program signal to program the datum into the selected memory cell; a first erase verify device having a first input connected to receive the input datum, a second input connected to the output of the first read circuit, and an

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output that supplies an erase verify signal having a value that reflects whether the input datum is equal to the datum read by the first read circuit".

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tran et al. (Patent No.: US 6,519,180 B2) discloses a verify-program cycle includes a verify cycle followed by a program cycle. A verify cycle is done first to inhibit the cell from the first programming pulse if the cell is verified, therefore preventing possible over-programming.

Di Zenzo et al. (Pub. No.: US 2003/0101390 A1) disclose a full internal erase-erase check algorithm involves many steps such as Pre-program, Pre-program Verify, Erase Verify, Erase, Depletion check, Compaction, Erase Verify.

9. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

10. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or

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proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 12/14/2004